

## CLAIMS

- 1           1. A system comprising:  
2           shared system registers, each register including an access protocol and data; and  
3           N processors,  $N \geq 2$ , where N is an integer, each accessing the registers.
- 1           2. A system, as defined in claim 1, the access protocol including a configurable  
2           access type for each N processors.
- 1           3. A system, as defined in claim 2, the access type being selected from a group  
2           that includes READ, READ/CLEAR, READ/SET, and READ/WRITE.
- 1           4. A system as defined in claim 3, comprising programmable configuration  
2           registers operative to encode and store the access protocol, each configuration register  
3           corresponding to one of the shared system registers.
- 1           5. A system, as defined in claim 4, wherein:  
2           each programmable configuration register consisting of  $N*2$  bits; and  
3           the configurable access types are encoded into 2 bits.
- 1           6. A system as defined in claim 3, the access protocol encoded and provided as  
2           input signals to the hardware design.
- 1           7. A system, as defined in claim 3, the access protocol encoded and selected as a  
2           build-time option in the hardware design source code.
- 1           8. A system, as defined in claim 3, the access protocol further including an  
2           arbitration priority.
- 1           9. A system as defined in claim 8, comprising programmable configuration  
2           registers operative to encode and store the access protocol, each configuration register  
3           corresponding to one of the shared system registers.

1           10. A system, as defined in claim 9, wherein:  
2           N is 2; and  
3           each programmable register including 5-bits, 2 bits represent the access type of  
4 one of the two processors, 2 bits represent the access type of the other of the two  
5 processors, and 1 bit represents the arbitration priority.

1           11. A system, as defined in claim 9, wherein:  
2           each programmable configuration registers consists of  $N \cdot (2 + \text{ceiling}(\log_2 N))$   
3 bits; and  
4           the access protocol including the four access types are encoded into 2 bits per  
5 processor and the arbitration priority encoded into  $\text{ceiling}(\log_2 N)$  bits.

1           12. A system, as defined in claim 8, the access protocol encoded and selected as a  
2 build-time option in the hardware design source code.

1           13. A system as defined in claim 8, the access protocol encoded and provided as  
2 input signals to the hardware design.